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Eindhoven (NL). **DE JONG, Franciscus, G., M.** [NL/NL];
c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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(74) Agent: **DULJVESTIJN, Adrianus, J.**; Philips Intellectual
Property & Standards, Prof. Holstlaan 6, NL-5656 AA
Eindhoven (NL).

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(71) Applicant (*for all designated States except US*): **KONIN-
KLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

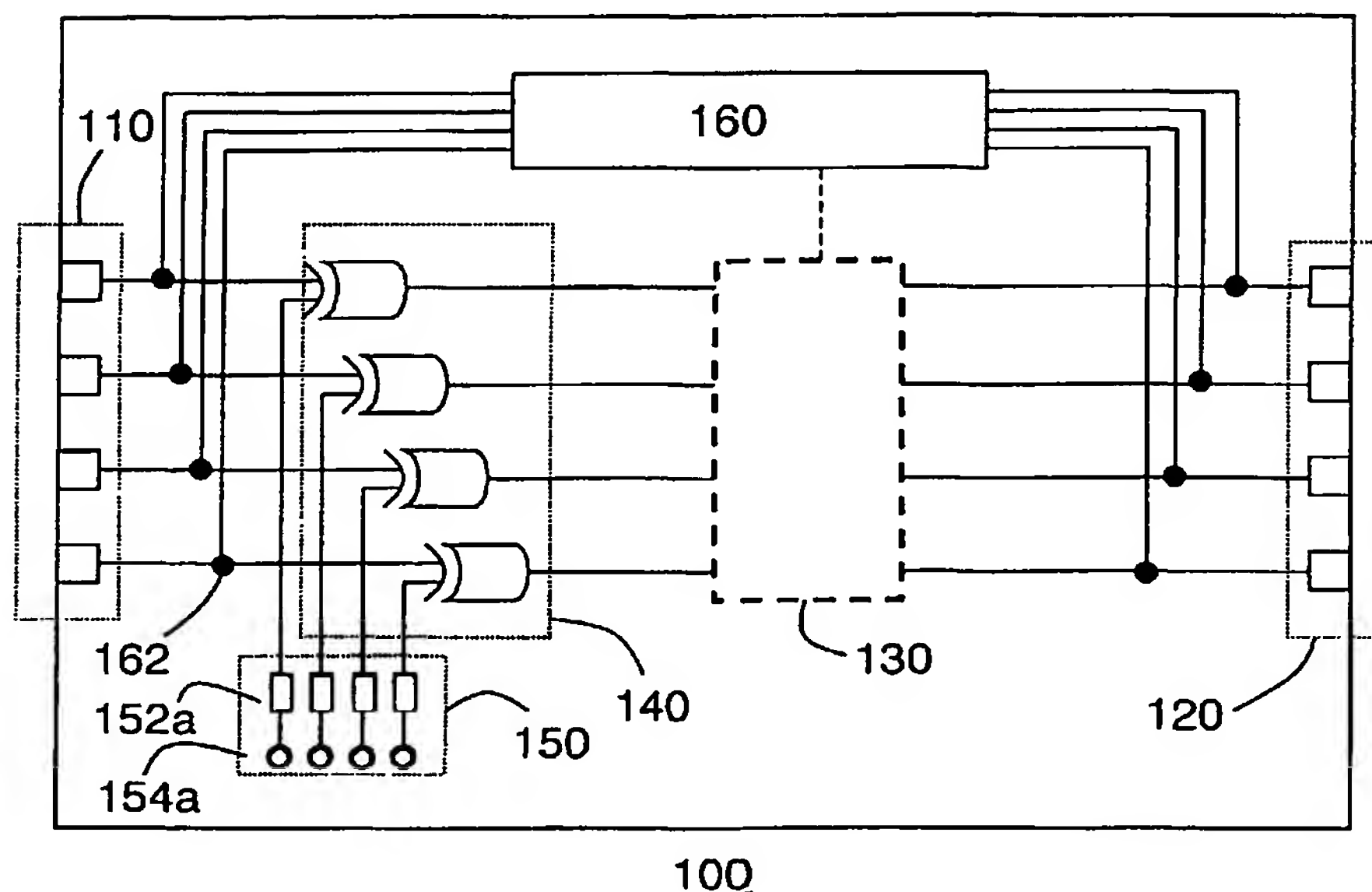
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(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **VAN DE LOGT,**
Leon, M., A. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA

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(54) Title: INTEGRATED CIRCUIT WITH EMBEDDED IDENTIFICATION CODE



(57) Abstract: An integrated circuit (100) has a plurality of inputs (110) and a plurality of outputs (120). In a test mode, a test arrangement including a plurality of logic gates (140) is coupled between the plurality of inputs (110) and the plurality of outputs (120). The logic gates from the plurality of logic gates (140) have a first input coupled to an input of the plurality of inputs (110) and a further input coupled to a fixed logic value source (150). The fixed logic value source (150) is used to define an identification code of the integrated circuit (100), which can be retrieved at the plurality of outputs (120) when an appropriate bit pattern is fed to the plurality of inputs (110).



Declaration under Rule 4.17:

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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 289 113 A (SPEER RAYMOND J ET AL) 22 February 1994 (1994-02-22) claim 1	1
A	EP 1 083 435 A (FUJITSU LTD) 14 March 2001 (2001-03-14) claims 1,2	1



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Patent family members are listed in annex.

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European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

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Information on patent family members

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			JP	5501153 T	04-03-1993
			WO	9102258 A1	21-02-1991
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